What is claimed is:

1. A package for holding at least two integrated circuits comprising:
an upper board and a lower board, the lower surface of the upper board being bonded to the upper surface of the lower board by a set of electrically conductive bonding members, in which;
said upper board has a set of upper contact members adapted for bonding an upper integrated circuit through signal-carrying contacts formed on an upper surface of said upper board in an upper integrated circuit location;
said upper board has a bonding surface on said lower surface thereof below said upper integrated circuit location;
said lower board has an aperture passing therethrough below said bonding surface, thereby forming a cavity adapted for holding a lower integrated circuit; and
said lower board has a set of wirebond pads disposed about said aperture on a lower surface of said lower board for contacting said second integrated circuit.

2. A package according to claim 1, in which there is at least one electrically conductive path from one of said set of upper contact members through one of said electrically conductive bonding members to one of said set of wirebond pads, thereby establishing a short signal path between said upper integrated circuit and said lower integrated circuit.

3. A package according to claim 1, in which said lower integrated circuit projects below said lower surface of said upper board by an offset distance comprising the thickness of bonding material between said lower integrated

circuit and said upper board plus the thickness of said lower integrated circuit, and in which said offset distance extends past said lower surface of said lower board by an offset difference, whereby a connection between said lower surface of said lower board and a support surface need only be greater than said offset distance.

4. A package according to claim 2, in which said lower integrated circuit projects below said lower surface of said upper board by an offset distance comprising the thickness of bonding material between said lower integrated circuit and said upper board plus the thickness of said lower integrated circuit, and in which said offset distance extends past said lower surface of said lower board by an offset difference, whereby a connection between said lower surface of said lower board and a support surface need only be greater than said offset distance.

5. A package according to claim 1, in which an upper integrated circuit is bonded to said set of upper contact members, a rim is bonded to said upper surface of said upper board and a lid is bonded to an upper surface of said rim, thereby enclosing said upper integrated circuit; and
said lower integrated circuit is encapsulated by encapsulating material, thereby reducing the amount of clearance needed below said lower board.

6. A package according to claim 2, in which an upper integrated circuit is bonded to said set of upper contact members, a rim is bonded to said upper surface of said upper board and a lid is bonded to an upper surface of said rim, thereby enclosing said upper integrated circuit; and

said lower integrated circuit is encapsulated by encapsulating material, thereby reducing the amount of clearance needed below said lower board.

7. A package according to claim 3, in which an upper integrated circuit is bonded to said set of upper contact members, a rim is bonded to said upper surface of said upper board and a lid is bonded to an upper surface of said rim, thereby enclosing said upper integrated circuit; and
said lower integrated circuit is encapsulated by encapsulating material, thereby reducing the amount of clearance needed below said lower board.

8. A package according to claim 1, in which said lower board has a set of electrically conductive bonding members in a pattern adapted for bonding with a counterpart set on said lower surface of said upper board and a set of wirebond pads on said lower surface of said lower board adapted for carrying signals to an nth integrated circuit of a group of integrated circuits compatible with said upper integrated circuit, whereby said upper board may be bonded to one of a set of lower boards, each compatible with a different lower integrated circuit, so that said upper integrated circuit may be combined with any of said group of integrated circuits compatible with said upper integrated circuit.

9. A package according to claim 2, in which said lower board has a set of electrically conductive bonding members in a pattern adapted for bonding with a counterpart set on said lower surface of said upper board and a set of wirebond pads on said lower surface of said lower board adapted for carrying signals to an nth integrated circuit of a group of integrated circuits compatible with said upper integrated circuit, whereby said upper board

may be bonded to one of a set of lower boards, each compatible with a different lower integrated circuit, so that said upper integrated circuit may be combined with any of said group of integrated circuits compatible with said upper integrated circuit.

10. A package according to claim 3, in which said lower board has a set of electrically conductive bonding members in a pattern adapted for bonding with a counterpart set on said lower surface of said upper board and a set of wirebond pads on said lower surface of said lower board adapted for carrying signals to an nth integrated circuit of a group of integrated circuits compatible with said upper integrated circuit, whereby said upper board may be bonded to one of a set of lower boards, each compatible with a different lower integrated circuit, so that said upper integrated circuit may be combined with any of said group of integrated circuits compatible with said upper integrated circuit.

11. A method of forming a package for integrated circuits comprising the steps of:

forming an upper board having a set of upper contact members adapted for bonding an upper integrated circuit through signal-carrying contacts formed on an upper surface of said upper board in an upper integrated circuit location and a set of electrically conductive bonding members on a lower surface of said upper board, said upper board having a bonding surface on said lower surface thereof below said upper integrated circuit location; forming a lower board having a counterpart set of electrically conductive bonding members on an upper surface of said upper board matching said set

of electrically conductive bonding members on said lower surface of said upper board and having an aperture passing therethrough below said bonding surface, thereby forming a cavity adapted for holding a lower integrated circuit and a set of wirebond pads disposed about said aperture on a lower surface of said lower board for contacting said second integrated circuit; and

bonding said upper board to said lower board with said set of electrically conductive bonding members.

12. A method of forming a package for integrated circuits according to claim 11, further comprising the steps of:

bonding an upper integrated circuit to said upper board and testing the combination of said upper integrated circuit and said upper board;

bonding a lower integrated circuit to said lower board and testing the combination of said lower integrated circuit and said lower board; and

thereafter bonding said upper board to said lower board.